36/3,K/124 (Item 124 from file: 347)
DIALOG(R)File 347:JAPIO

01457382 **Image available**
DATA PROTECTING SYSTEM

PUB. NO.: 59-168982 [JP 59168982 A]
PUBLISHED: September 22, 1984 (19840922)
INVENTOR(s): HIROKAWA KATSUHISA
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-044708 [JP 8344708]
FILED: March 17, 1983 (19830317)
JOURNAL: Section: P, Section No. 331, Vol. 09, No. 24, Pg. 134, January 31, 1985 (19850131)

JAPIO CLASS: 45.2 (INFORMATION **PROCESSING** -- **Memory** ...

...Memory Units)
JAPIO KEYWORD:R131 (INFORMATION **PROCESSING** --

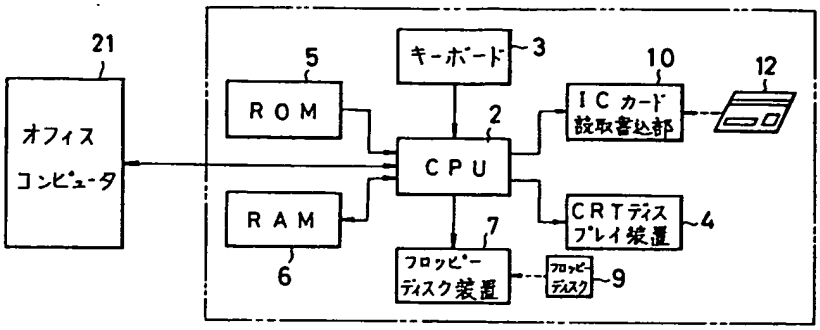
ABSTRACT

PURPOSE: To protect contents of recording and to prevent destruction by **detecting** extraction of recording medium according to a signal from a **connector** and operating destruction preventing sequence of a built-in **memory** .

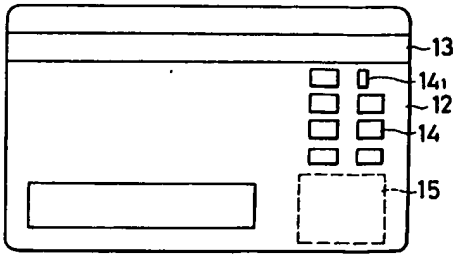
...

...CONSTITUTION: When an **IC card** 12 is extracted by mistake, a **connector** 14 becomes non-connecting state with an **IC chip** readig and writing device earlier than other **connectors** . Then, a fall **detecting** circuit 18 **detects** fall according to a signal from the **connector** 14, and the **detection** signal is outputted to an FF circuit 19. Thus, the supply of a chip selection signal from a CPU16 to an ROM17 is **stopped** . Consequently, the reading or writing is not performed simultaneously with extraction of the **IC card** , and the contents of **memory** of ROM17 are protected from becoming erroneous one, and destruction of **ROM** is prevented.

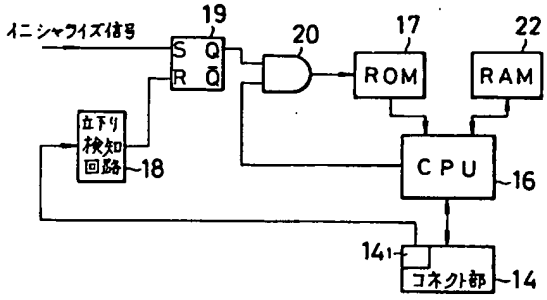
第 3 図



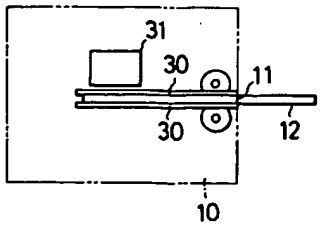
第 4 図



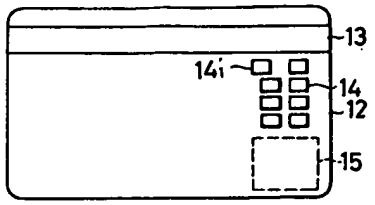
第 5 図



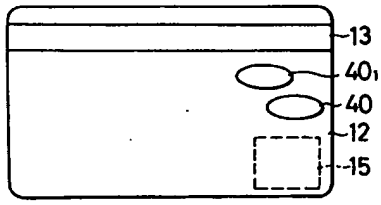
第 6 図



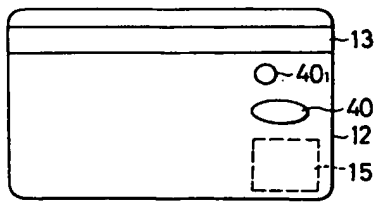
第 7 図



第 8 図



第 9 図



```
Set     Items   Description
S1          7   (MONOLITH? OR INTEGRAT?)(2N)SECURITY()MODULE?
S2      15058   SMARTCARD? OR SMART()CARD? ? OR ICCARD? OR CHIPCARD? OR (C-
             HIP OR IC OR INTEGRATED?()CIRCUIT?)()CARD? ?
S3          1   (SEMICONDUCT? OR SEMI()CONDUCT?)()CARD? ?
S4   15480485   CHECK? OR MONITOR? OR TEST? OR AUDIT? OR TRACK? OR MEASUR?
             OR ASSESS? OR ASCERTAIN?
S5    8549818   EVALUAT? OR SENSOR? OR TRANSDUC? OR SENSING? OR DETECT? OR
             COMPARATOR?
S6       8893   DATABUS? OR DATA()(BUS OR BUSES OR BUSSES)
S7      85309   PCI? ? OR ISA? ? OR EISA? ? OR VLBUS? OR AGP? ? OR USB? ? -
             OR MCA? ? OR VESABUS? OR VESALOCAL?
S8     291974   CONDUCTOR? OR (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC -
             OR DATA?)(2N)(PATH? OR VIA? ? OR CONNECTION?)
S9      48772   DATA()TRANSMITTER? OR CONNECTOR?
S10    129086   (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(-
             TRACK? OR LANE? OR CHANNEL? OR PORT? OR INTERCONNECT?)
S11    848846   PROCESSOR? OR ICCHIP? OR IC()CHIP? OR INTEGRATED()CIRCUIT?
             OR CPU? ?
S12   3060874   DATAPROCESSOR? OR MICROPROCESSOR? OR PROCESSING? OR MICROC-
             ONTROLLER? OR (MICRO OR LOGIC)()CONTROLLER?
S13    958343   MEMOR? OR RAM? ? OR VRAM? ? OR NVRAM? ? OR ROM? ? OR PROM?
             ?
S14     60442   EPROM? ? OR EEPROM? ? OR ICMEMOR? OR CHIPMEMOR? OR SRAM? OR
              DRAM? ?
S15    470991   DISABL? OR DISCONNECT? OR DISARM? OR INCAPACITAT? OR CRIPP-
             L? OR TAMPER? OR IMPAIR? OR DEBILITAT?
S16    979173   STOP? OR ARREST? OR CEASE? OR CESSAT? OR CEASING? OR BLOCK-
             ING? OR INTERRUPT? OR IMMOBIL? OR DEACTIVAT?
S17     44341   RANDOM?(5N)(GENERAT?)
S18     17857   (PARITY OR EQUIVALENT? OR EQUAL? OR IDENTICAL?)(5N)GENERAT?
S19      1256   ANTITAMPER? OR ANTIHACK? OR ANTI()(TAMPER? OR HACK?) OR (T-
             AMPER? OR HACK?)()(PROOF OR RESISTANT?)
S20        75   S1:S3 AND S6:S10 AND S11:S12 AND S13:S14
S21        30   S20 AND (S4:S5 OR S15:S19)
S22        75   S20:S21
S23        58   S22 AND PY<2002
S24        56   RD (unique items)
File   2:INSPEC 1898-2005/Nov W3
         (c) 2005 Institution of Electrical Engineers
File   6:NTIS 1964-2005/Nov W3
         (c) 2005 NTIS, Intl Cpyrght All Rights Res
File   8:Ei Compendex(R) 1970-2005/Nov W3
         (c) 2005 Elsevier Eng.  Info. Inc.
File  34:SciSearch(R) Cited Ref Sci 1990-2005/Nov W3
         (c) 2005 Inst for Sci Info
File  35:Dissertation Abs Online 1861-2005/Nov
         (c) 2005 ProQuest Info&Learning
File  65:Inside Conferences 1993-2005/Nov W4
         (c) 2005 BLDSC all rts. reserv.
File  94:JICST-EPlus 1985-2005/Sep W4
         (c)2005 Japan Science and Tech Corp(JST)
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Oct
         (c) 2005 The HW Wilson Co.
File 111:TGG Natl.Newspaper Index(SM) 1979-2005/Nov 30
         (c) 2005 The Gale Group
File 144:Pascal 1973-2005/Nov W3
         (c) 2005 INIST/CNRS
File 239:Mathsci 1940-2005/Jan
         (c) 2005 American Mathematical Society
File 256:TecInfoSource 82-2005/Feb
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36/3,K/76 (Item 76 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007095330
WPI Acc No: 1987-095327/198714
XRPX Acc No: N87-071637
Integrated circuit card **esp. credit card** - disconnects test **address or data terminals from bus after** memory test **has been completed**
Patent Assignee: CASIO COMPUTER CO LTD (CASK)
Inventor: HARA K; KAWANA S; NAKANO H
Number of Countries: 004 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
EP 217281	A	19870408	EP 86113130	A	19860924	198714 B
US 4845351	A	19890704	US 86909217	A	19860918	198934
EP 217281	B	19910227				199109
DE 3677686	G	19910404				199115
EP 217281	B2	19950426	EP 86113130	A	19860924	199521

Priority Applications (No Type Date): JP 85237134 A 19851023; JP 85216743 A 19850930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 217281	A	E	14		
Designated States (Regional): DE FR GB					
US 4845351	A		12		
EP 217281	B				
Designated States (Regional): DE FR GB					
EP 217281	B2	E	14	G06K-019/073	
Designated States (Regional): DE FR GB					

Integrated circuit card **esp. credit card**...

... disconnects test **address or data terminals from bus after** memory test **has been completed**

...Abstract (Basic): The I.C. card comprises a **memory** such as an **EEPROM** (22) which stores secret data such as a PIN. The **test** address terminals (A1..Am) of the cord are connected for **testing** the **memory** to an address bus (26) of the **EEPROM** . The **test** data terminals (Di ...

...Abstract (Equivalent): An **integrated circuit card** comprising data input/output terminal means (I/O); **memory** means (22,165) wherein direct access to at least a portion of the **memory** means (22,165) is prevented, said **memory** means storing secret data when input to said **memory** means through said data input/output terminal means (I/O), said **memory** means (22, 165) being arranged to output the secret data in response to an access command made indirectly **via** the **data** input/output terminal means (I/O); an address bus (26) and a **data bus** (24) associated with said **memory** means (22,165); **test** address terminals (A1-Am) connected to the address bus (26) of said **memory** means (22,165), for enabling addresses of the **memory** means to be accessed during a **test** operation; **test** data terminals (D1-Dn) arranged to be connected to the **data bus** (24) of said **memory** means (22,165), for enabling inputting of data to and outputting of data from the **memory** means during said **test** operation; and the **test** address terminals (A1-Am) being **disconnected** from the address bus (26) and/or the **test** data terminals (D1-Dn) being **disconnected**

the **data bus** (24) after the completion of the **test** operation, characterised by **comparator** means (168) for comparing an address input **via** the **data** input/ output terminal means (I/O) with a predetermined address, and for generating a coincidence signal upon agreement; and gate means (181) coupled between at least one of said **test** data terminals (D1-Dn) and said **data bus** (24) and/or between said **test** address terminals (A1-Am) and said address bus (26), for **disconnecting** at least one of the **test** terminals when the coincidence signal of said **comparator** means (168) is present, whereby after the completion of said **test** operation even when the access command is applied to said **test** address terminals (A1-Am), said secret data is thus unobtainable from said **test** data terminals (D1-Dn). (16pp)

...Abstract (Equivalent): An IC including an EEP- **ROM** is formed on a semiconductor wafer. The IC also has exposed address pads connected to the address bus of the EEP- **ROM** , and exposed data pads connected to the **data bus** of the EEP- **ROM** . A **test** probe is brought into contact with these pads, performing various **tests** on the IC. After the IC has been **tested** , the wafer is diced into IC pellets. The address pads are **disconnected** from the address bus and/or the data pads are **disconnected** from the **data bus** .

...

...For example, the edge **portions** of the **IC** pellet on which the address pads and/or the data pads are formed are cut by dicing from the remaining **portion** of the **IC** pellet. The connecting pads of the IC pellet are wire-bonded to leads, and the...

...pellet is sealed with a resin. Finally, the sealed IC pellet is built in an **IC card** body. (12pp)

...Title Terms: **DISCONNECT** ;

United States Patent [19]

Hara et al.

[11] **Patent Number: 4,845,351**

[45] **Date of Patent: Jul. 4, 1989**

[54] **IC CARD**

[75] Inventors: **Kazuya Hara; Harumi Nakano; Shigeyuki Kawana, all of Tokyo, Japan**

[73] Assignee: **Casio Computer Co., Ltd., Tokyo, Japan**

[21] Appl. No.: **909,217**

[22] Filed: **Sep. 18, 1986**

[30] **Foreign Application Priority Data**

Sep. 30, 1985 [JP] Japan 60-216743
Oct. 23, 1985 [JP] Japan 60-237134

[51] **Int. Cl.**[4] **G06K 19/06**
[52] **U.S. Cl.** **235/492**; 235/438; 235/487
[58] **Field of Search** 235/487, 492, 438

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,971,916	7/1976	Moreno	235/61.7 B
4,105,156	8/1978	Dethloff	235/487 X
4,446,475	5/1984	Gercekci et al.	235/487 X
4,572,946	2/1986	Schrenk	235/492 X
4,650,975	3/1987	Kitchener	235/492 X
4,697,073	9/1987	Hara	235/487

FOREIGN PATENT DOCUMENTS

0172108	2/1986	European Pat. Off.	235/492
8300244	1/1983	PCT Int'l Appl. .	

OTHER PUBLICATIONS

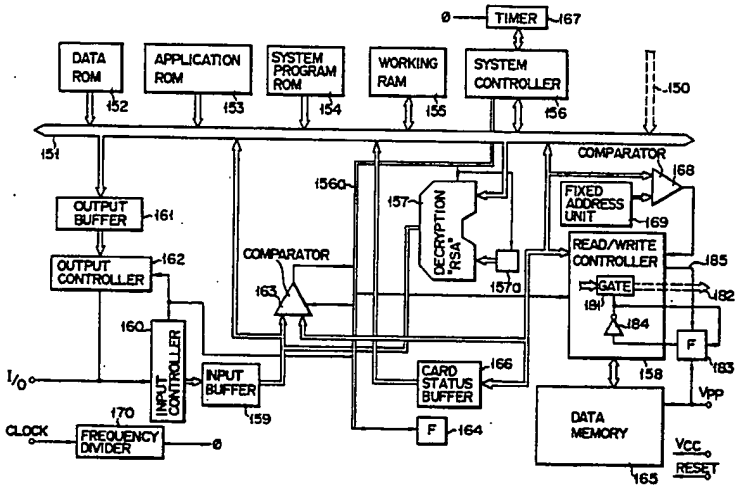
IEEE Spectrum, vol. 21, No. 2, Feb. 1984; pp. 43–49.

Primary Examiner—Patrick R. Salce
Assistant Examiner—Marc S. Hoff
Attorney, Agent, or Firm—Frishauf, Holtz, Goodman & Woodward

[57] **ABSTRACT**

An IC including an EEP-ROM is formed on a semiconductor wafer. The IC also has exposed address pads connected to the address bus of the EEP-ROM, and exposed data pads connected to the data bus of the EEP-ROM. A test probe is brought into contact with these pads, thereby performing various tests on the IC. After the IC has been tested, the wafer is diced into IC pellets. The address pads are disconnected from the address bus and/or the data pads are disconnected from the data bus. For example, the edge portions of the IC pellet on which the address pads and/or the data pads are formed are cut by dicing from the remaining portion of the IC pellet. Thereafter, the connecting pads of the IC pellet are wire-bonded to leads, and the IC pellet is sealed with a resin. Finally, the sealed IC pellet is built in an IC card body.

5 Claims, 6 Drawing Sheets



been tested. Alternatively, all test pads are disconnected from the data line and address line after the test of the IC pellet. Therefore, an illegal access to the data memory provided within the IC card is prevented, ensuring not only the security of the IC card, but also that of the IC card system.

The present invention is not limited to the embodiments described above. Various changes and modifications can be made, without departing from the spirit of this invention.

What is claimed is:

1. An integrated circuit (IC) card, comprising:

data input/output terminal means;

memory means for storing secret data when inputted to said memory means through said data input/output terminal means, said memory means being arranged to output the secret data in response to an access command;

an address bus and a data bus each associated with said memory means;

identification means for identifying data inputted via said data input/output terminal means with the secret data stored in said memory means, and for generating a coincidence signal;

test address terminals connected to the address bus of said memory means, for enabling addresses of the memory means to be accessed during a test operation;

test data terminals arranged to be connected to the data bus of said memory means, for enabling inputting of data to and outputting of data from the memory means during said test operation;

detecting means for detecting a completion of the test operation for said memory means; and

switching means coupled between said test data terminals and said data bus, for connecting said data bus with said test data terminals until said detecting means detects the completion of said test operation, and for disconnecting said data bus from said test data terminals when the completion of the test operation is detected;

wherein said memory means is non-responsive to said access command when the access command is applied to said test address terminals and the secret data is thus unobtainable from said test data terminals, after completion of said test operation.

2. An IC card according to claim 1, in which said switching means comprises a flag section set upon completion of the test of said memory means, first gate means connecting said test address terminals to the address bus of the memory means and second gate means connecting said data terminals to the data bus of the memory means, and at least one of said first gate means and second gate means being turned off in accordance with the value of the output of the flag section.

3. An IC card according to claim 1, further comprising data clearing means for clearing the secret data stored in said memory means.

4. An IC card according to claim 3, in which said data-clearing means comprises an address memory for storing an unused address of said memory means, comparator means for comparing a memory address input to achieve an access to said memory means, with the unused memory address stored in said address memory, and means for clearing the data stored in said memory means, when the input address is found to be identical with the unused address.

5. A method of manufacturing an integrated circuit (IC) card, comprising the steps of:

providing integrated circuit means having memory means for storing secret data;

connecting data input/output means to the memory means;

connecting test address terminals to an address bus associated with the memory means;

arranging test data terminals for connection to a data bus associated with the memory means;

providing detecting means for detecting the completion of a test operation for the memory means;

connecting switching means between said data bus and said test data terminals;

detecting the completion of the test operation with the detecting means by using the test address terminals for said memory means;

disconnecting the data bus of the memory means from the test data terminals by turning off the switching means upon detecting the completion of the test operation;

arranging the integrated circuit means in casing means; and

writing secret data in the memory means.

* * * * *

36/3,K/106 (Item 106 from file: 347)
DIALOG(R)File 347:JAPIO

02773292 **Image available**
IC CARD READER/WRITER

PUB. NO.: 01-070892 [JP 1070892 A]
PUBLISHED: March 16, 1989 (19890316)
INVENTOR(s): MATSUMURA SHUICHI
APPLICANT(s): DAINIPPON PRINTING CO LTD [000289] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 62-226438 [JP 87226438]
FILED: September 11, 1987 (19870911)
JOURNAL: Section: P, Section No. 892, Vol. 13, No. 284, Pg. 116, June 29, 1989 (19890629)

IC CARD READER/WRITER
JAPIO CLASS: 45.3 (INFORMATION **PROCESSING** --
JAPIO KEYWORD:R131 (INFORMATION **PROCESSING** --

ABSTRACT
...of a fault at the time of generating abnormality, to protect the data of an **IC card** from being broken, and to make it possible to use the device also for an **IC card** including an **EPROM** by using a battery for the power supply of the device and providing various **monitoring** circuits, **comparators** or the like...

...supply of the device is boosted by a boosting circuit 3 and impressed to an **IC card** power supply voltage terminal 19 through a regulator 7 or the like. On the other hand, a voltage boosted by a boosting circuit 2 is impressed to an **IC card** data writing voltage impressing terminal 18 through a data writing voltage switching circuit 4 to drive the **IC card** . Data transmitted/received through a data reading/writing terminal 21 are transferred through external device through a data transfer means (a signal interinterruption circuit 14, a **microprocessor** 15, etc.), and when the voltage drop of a power supply voltage or a data writing voltage is **detected** by voltage **monitoring** circuits 10, 11 or an excess current is **detected** by **comparators** 8, 9, 13, all terminals other than a ground terminal are **disconnected** . Consequently, the device can be made convenient for **portable** use and **data** can be prevented from being broken at the time of generating abnormality.

36/3,K/97 (Item 97 from file: 347)
DIALOG(R)File 347:JAPIO

03100692 **Image available**
IC CARD READER

PUB. NO.: 02-076192 [JP 2076192 A]
PUBLISHED: March 15, 1990 (19900315)
INVENTOR(s): SAKAMOTO HIROSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-228211 [JP 88228211]
FILED: September 12, 1988 (19880912)
JOURNAL: Section: P, Section No. 1059, Vol. 14, No. 269, Pg. 64, June 11, 1990 (19900611)

IC CARD READER
JAPIO CLASS: 45.2 (INFORMATION **PROCESSING** -- **Memory** ...

...Memory Units); 45.3 (INFORMATION PROCESSING --
JAPIO KEYWORD:R131 (INFORMATION **PROCESSING** --

ABSTRACT
PURPOSE: To beforehand prevent the runaway of a CPU by inputting an **interrupting** signal due to the software into a central **processing** unit (CPU) when an **IC card** is removed from a **connector** .

...

...CONSTITUTION: Since an electrode 13-3 for **detecting** a card is first separated from an electrode in a **connector** part 1 at the time of removing an **IC card** , when an address signal, a data signal and a command signal transmitted by a signal electrode 13-4 is effective, the difference between a card **detecting** latch signal (b) and a card **detecting** signal (a) due to a **comparator** 3 is **detected** . An **interrupting** selector signal (c) is active, hardware **interruption** is applied to a CPU 7 and simultaneously, the signal (c) is also inputted to a selector circuit 4. Then, the selector circuit 4 selects a main **data bus** (f) and the software **interrupting** code is read from a fixed data output machine 6, the software **interruption** is applied and the **processing** of the **interruption** routine is executed. Thus, the runaway of the CPU 7 is prevented beforehand.

```
Set     Items   Description
S1          6   (MONOLITH? OR INTEGRAT?)(2N)SECURITY()MODULE?
S2      38647   SMARTCARD? OR SMART()CARD? ? OR ICCARD? OR CHIPCARD? OR (C-
             HIP OR IC OR INTEGRATED?()CIRCUIT?)()CARD? ?
S3        100   (SEMICONDUCT? OR SEMI()CONDUCT?)()CARD? ?
S4    2680677   CHECK? OR MONITOR? OR TEST? OR AUDIT? OR TRACK? OR MEASUR?
             OR ASSESS? OR ASCERTAIN?
S5    2866349   EVALUAT? OR SENSOR? OR TRANSDUC? OR SENSING? OR DETECT? OR
             COMPARATOR?
S6      23576   DATABUS? OR DATA()(BUS OR BUSES OR BUSSES)
S7      13788   PCI? ? OR ISA? ? OR EISA? ? OR VLBUS? OR AGP? ? OR USB? ? -
             OR MCA? ? OR VESABUS? OR VESALOCAL?
S8     512125   CONDUCTOR? OR (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC -
             OR DATA?)(2N)(PATH? OR VIA? ? OR CONNECTION?)
S9     309546   DATA()TRANSMITTER? OR CONNECTOR?
S10    134126   (ELECTRIC? OR ELECTRONIC? OR CIRCUIT? OR IC OR DATA?)(2N)(-
             TRACK? OR LANE? OR CHANNEL? OR PORT? OR INTERCONNECT?)
S11    682784   PROCESSOR? OR ICCHIP? OR IC()CHIP? OR INTEGRATED()CIRCUIT?
S12   2166640   DATAPROCESSOR? OR MICROPROCESSOR? OR PROCESSING? OR MICROC-
             ONTROLLER? OR (MICRO OR LOGIC)()CONTROLLER?
S13   1124912   MEMOR? OR RAM? ? OR VRAM? ? OR NVRAM? ? OR ROM? ? OR PROM?
             ? OR EPROM? ? OR EEPROM? ? OR ICMEMOR? OR CHIPMEMOR?
S14    216942   DISABL? OR DISCONNECT? OR DISARM? OR INCAPACITAT? OR CRIPP-
             L? OR TAMPER? OR IMPAIR? OR DEBILITAT?
S15   1161490   STOP? OR ARREST? OR CEASE? OR CESSAT? OR CEASING? OR BLOCK-
             ING? OR INTERRUPT? OR IMMOBIL?
S16     19092   (PARITY? OR RANDOM?)(5N)(GENERAT?)
S17       360   ANTITAMPER? OR ANTIHACK? OR ANTI()(TAMPER? OR HACK?)
S18   1568531   IC=(G06F? OR H04L?)
S19   1344638   MC=(T01? OR W01?)
S20      1248   S1:S3 AND S6:S10 AND S11:S12 AND S13
S21        39   S20 AND S4:S5 AND S14:S15
S22        13   S20 AND S16
S23         0   S20 AND S17
S24        15   S20 AND S14:S15(7N)S6:S10
S25        87   S20 AND S4:S5(7N)S6:S10
S26       294   S1:S3 AND S6:S13 AND S16
S27       251   S26 AND S18:S19
S28         9   S26:S27 AND (S4:S5 OR S14:S15) AND S6:S10 AND S11:S13
S29        62   S21:S22 OR S24 OR S28
S30        16   S29 AND S25
S31        62   S29:S30
S32    830707   PR=2002:2005
S33        57   S31 NOT S32
S34        67   S25 NOT S31:S32
S35       124   S33:S34
S36       124   IDPAT (sorted in duplicate/non-duplicate order)
File 347:JAPIO Nov 1976-2005/Jul(Updated 051102)
        (c) 2005 JPO & JAPIO
File 350:Derwent WPIX 1963-2005/UD,UM &UP=200576
        (c) 2005  Thomson Derwent
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S16	1598	S12 or S13 or S14 or S15	USPAT	OR	OFF	2005/11/04 13:46
S17	501	S16 and (monolithic or chip or smart or ic or integrated adj circuit) adj card$1	USPAT	OR	OFF	2005/11/04 13:47
S18	13	S17 and (check$4 or detect$4) near3 bus$3	USPAT	OR	OFF	2005/11/04 13:49
S19	0	S17 and radiation with hack$3	USPAT	OR	OFF	2005/11/04 13:50
S20	0	S16 and radiation with hack$3	USPAT	OR	OFF	2005/11/04 14:37
S21	63	S16 and radiation	USPAT	OR	OFF	2005/11/04 14:08
S22	58	S16 and instruction near3 code$1	USPAT	OR	OFF	2005/11/04 14:09
S23	8	S22 and (set or building or defin$4) near4 module	USPAT	OR	OFF	2005/11/04 14:14
S24	14633	(monilithic or chip or ic or smart or integrated adj circuit) adj card$1	USPAT	OR	OFF	2005/11/04 14:15
S25	0	S24 and operation adj code near4 execut$4 adj instruction	USPAT	OR	OFF	2005/11/04 14:17
S26	346	S24 and (operation adj code or execut$4 adj instruction)	USPAT	OR	OFF	2005/11/04 14:18
S27	0	S26 and (forbid$5 or prohibit$4) near3 values	USPAT	OR	OFF	2005/11/04 14:21
S28	323	S24 and (manufactur$4 or set) adj values	USPAT	OR	OFF	2005/11/04 14:22
S29	36	S26 and (manufactur$4 or set) adj values	USPAT	OR	OFF	2005/11/04 14:29
S30	18316	S24 and chang$4 execution adj (instruction or code$1)	USPAT	OR	OFF	2005/11/04 14:37
S31	0	S24 and (chang$4 or alter$4) near3 (execution adj (code or instruction$1))	USPAT	OR	OFF	2005/11/04 14:38
S32	7	S24 and (chang$4 or alter$4) near10 (execution adj (code or instruction$1))	USPAT	OR	OFF	2005/11/04 14:46
S33	193	S24 and instruction near10 table	USPAT	OR	OFF	2005/11/04 14:46
S34	167	S33 and (alter$4 or chang$4)	USPAT	OR	OFF	2005/11/04 14:47
S35	5	S34 and (alter$4 or chang$4) with value with (bus or memory)	USPAT	OR	OFF	2005/11/04 14:48
S36	1	data$1bus near3 transmi$4 near4 secure	USPAT	OR	OFF	2005/11/28 15:02
S37	1304	711/103,115.ccls.	USPAT	OR	OFF	2005/11/28 15:02
S38	0	S37 and ((smart or ic or chip) adj card$1 or monolithic) near3 data$1bbus near3 transmit$4 near4 secur$4	USPAT	OR	OFF	2005/11/28 15:06

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	724	non$1invasive adj technique	USPAT	OR	OFF	2005/12/01 18:09
L2	244666	(smart or iC) adj card or integrated adj circuit$1	USPAT	OR	OFF	2005/12/01 18:10
L3	244666	smart adj card or ic adj card or integrated adj circuit$1	USPAT	OR	OFF	2005/12/01 18:11
L4	107	l3 and current adj analysis	USPAT	OR	OFF	2005/12/01 18:14
L5	48	l4 and random$4	USPAT	OR	OFF	2005/12/01 18:14
L6	4	l4 and parity	USPAT	OR	OFF	2005/12/01 18:17
L7	492	l3 and parity adj generator	USPAT	OR	OFF	2005/12/01 18:17
L8	292	l7 and random$5	USPAT	OR	OFF	2005/12/01 18:18
L9	183	l8 and (sensor or detector or monitor)	USPAT	OR	OFF	2005/12/01 18:29
L10	164	l9 and (disabl$4 or disconnect$4)	USPAT	OR	OFF	2005/12/01 18:32
L11	102	l10 and clock adj signal	USPAT	OR	OFF	2005/12/01 18:32
L12	52	l11 and power adj up	USPAT	OR	OFF	2005/12/01 18:33
L13	51	l12 and @ad<"20010101"	USPAT	OR	OFF	2005/12/01 18:34
S1	1	"5442704".pn.	USPAT	OR	OFF	2005/11/04 12:22
S2	14247	(ic or smart or chip or monolithic) adj card$1	USPAT	OR	OFF	2005/11/04 12:24
S3	8179	S2 and detect$5	USPAT	OR	OFF	2005/11/04 12:24
S4	157	S2 and detect$5 with radiation	USPAT	OR	OFF	2005/11/04 12:25
S5	1	S2 and (intrus$5 or hack$4) with radiation	USPAT	OR	OFF	2005/11/04 12:34
S6	254	hazard.in.	USPAT	OR	OFF	2005/11/04 12:26
S7	3	S6 and security adj module	USPAT	OR	OFF	2005/11/04 12:26
S8	3	radiation with hacker$1	USPAT	OR	OFF	2005/11/04 12:39
S9	14	("5442704" "4281216" "4382279" "6536034" "4841131" "4930129" "5649129" "5649090" "6389536" "5826007" "5465349" "5819023" "6357046" "6357046" "5313618"). pn.	USPAT	OR	OFF	2005/11/04 13:24
S10	8	S9 and (monilithic or chip or ic or smart or integrated adj circuit) adj card$1	USPAT	OR	OFF	2005/11/04 14:15
S11	4	S9 and bus and detect$5	USPAT	OR	OFF	2005/11/04 12:55
S12	249	713/172.ccls.	USPAT	OR	OFF	2005/11/04 13:44
S13	555	713/193.ccls.	USPAT	OR	OFF	2005/11/04 13:44
S14	164	705/66,71.ccls.	USPAT	OR	OFF	2005/11/04 13:45
S15	713	380/28,66,71,172,193.ccls.	USPAT	OR	OFF	2005/11/04 13:46

S39	0	S37 and ((smart or ic or chip) adj card$1 or monolithic) near3 data$1bbus	USPAT	OR	OFF	2005/11/28 15:06
S40	0	S37 and ((smart or ic or chip) near3 card$1 or monolithic) near3 data$1bbus	USPAT	OR	OFF	2005/11/28 15:06
S41	0	S37 and (smart or ic or chip) adj card$1 near3 data$1bbus	USPAT	OR	OFF	2005/11/28 15:07
S42	139	S37 and (smart or ic or chip) adj card$1	USPAT	OR	OFF	2005/11/28 15:07
S43	1	S37 and (smart or ic or chip) adj card$1 with data$1bus	USPAT	OR	OFF	2005/11/28 15:07
S44	12	(smart or ic or chip) near3 card$1 with detect$4 with radiation	USPAT	OR	OFF	2005/11/28 15:10
S45	0	S44 and (data adj bus or data$1bus)	USPAT	OR	OFF	2005/11/28 15:09
S46	0	S44 and hacker$4	USPAT	OR	OFF	2005/11/28 15:10
S47	0	S37 and card$1 and radiation with (tamper$4 or detect$4 or hack$4 or modify$4 or attack$4)	USPAT	OR	OFF	2005/11/28 15:11
S48	3	S37 and radiation with (tamper$4 or detect$4 or hack$4 or modify$4 or attack$4)	USPAT	OR	OFF	2005/11/28 15:13
S49	1	secur$4 with transmit$5 with between with processor with (memory or storage$1) with card$1	USPAT	OR	OFF	2005/11/28 16:41
S50	14	("5978865" "5442704" "4281216" "4382279" "6536034" "4841131" "4930129" "5649090" "6389536" "4841131" "4930129" "5649090" "6389536" "589536" "5826007" "5465349" "5819023" "6357046" "5313618").pn.	USPAT	OR	OFF	2005/11/28 17:33
S51	13	S50 and (check or compar$4 or generat$5)	USPAT	OR	OFF	2005/11/28 17:33
S52	1	"5464349".pn.	USPAT	OR	OFF	2005/11/29 13:55
S53	1	"5465349".pn.	USPAT	OR	OFF	2005/11/29 13:55
S54	1	"5465349".pn.	USPAT	OR	OFF	2005/11/30 17:40
S55	0	S54 and data adj bus	USPAT	OR	OFF	2005/11/30 17:40
S56	0	S54 and bus3	USPAT	OR	OFF	2005/11/30 17:40
S57	1	"5442704".pn.	USPAT	OR	OFF	2005/11/30 18:54
S58	1	S57 and instruction	USPAT	OR	OFF	2005/11/30 18:56
S59	1	"5442704".pn.	USPAT	OR	OFF	2005/11/30 20:20
S60	0	S59 and access adj control adj microprocessor	USPAT	OR	OFF	2005/11/30 20:20

S61	0	S59 and access adj control near2 microprocessor	USPAT	OR	OFF	2005/11/30 20:21
S62	0	S59 and access near2 control near2 microprocessor	USPAT	OR	OFF	2005/11/30 20:21
S63	1	S59 and microprocessor	USPAT	OR	OFF	2005/11/30 20:26
S64	1	S59 and host and microprocessor	USPAT	OR	OFF	2005/11/30 20:26